

# PowerGrid Phase II – A Computation Engine for Large-Scale Electric Networks

## Peer Review Meeting

January 28, 2004

## Drexel University

- Chika Nwankpa
- Prawat Nagvajara
- Jeremy Johnson
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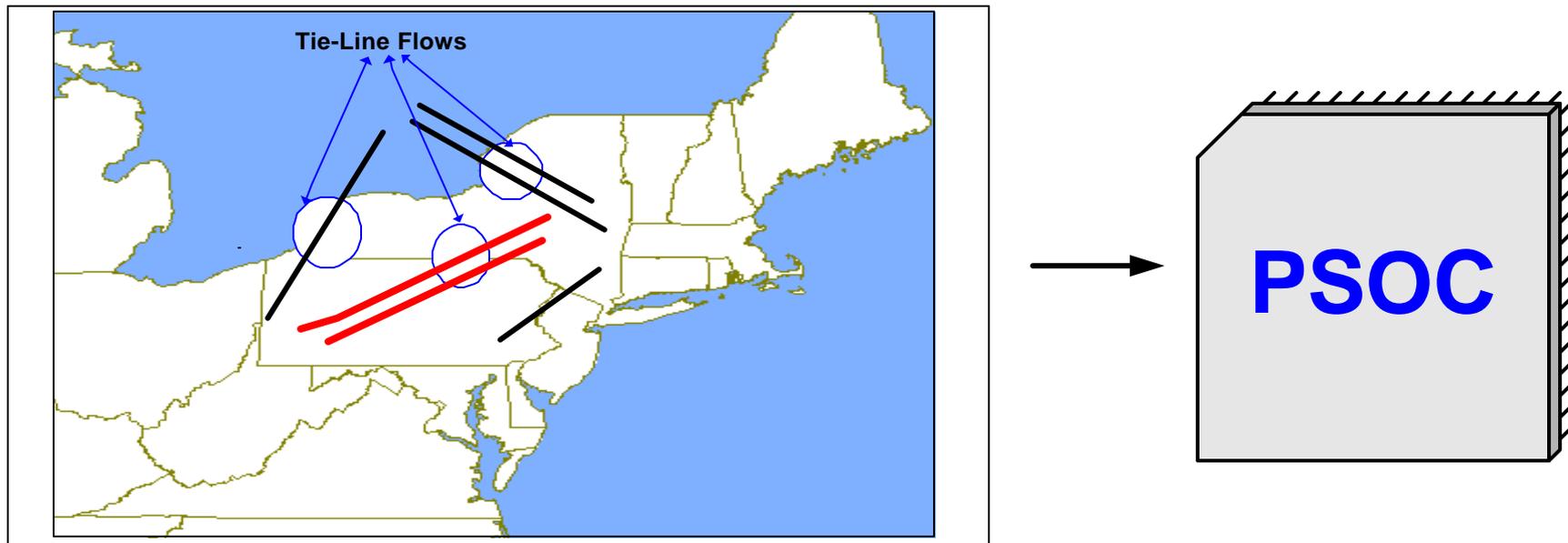
## NJIT

- Sotirios Ziavras

Herb Tate

- **Provide Benchmark data on power flow runs**
  - HW/SW environment (computer type, description of power flow runs)
  - Necessary I/O data
  - Timing information (CPU dependent)
- **Help identify strategies for successful development of PowerGrid Simulator**
  - What are the important/unimportant aspects of the PowerGrid?

## Power Grid Emulation Engine – Power System on a Chip (PSOC)



Features of PSOC:

1. Analog emulation of power system
2. Reconfigurable chips
3. Real-time computation of solution

## We have three stages to fully develop the PowerGrid Simulator:

- Digital Approach
- Analog Approach
- Mixed-signal (analog-digital) Approach

- Research concentrated on feasibility of an all Digital Approach to Power Flow computation.
  - Prototype hardware implementation of single contingency power-flow analysis
  - Designed and implemented a shared-memory parallel machine
  - Scalability analysis using performance model

- Commence work on Analog Approach
- Continue work on Digital Approach aimed at Implementation studies as it relates to:
  - Load Flows
  - Contingency Analysis
  - Economically Constrained Problems

- Perform Industrial Feasibility Study of All Digital Approach
- Perform Implementation Study of an All Analog Approach
- Examine intricate interdependencies between Digital and Analog approaches
- Commence work on Mixed-Signal Approach

# PowerGrid Project – Digital Approach

All-Digital System Approach to  
Large-scale Power System Analysis

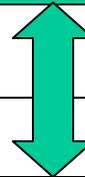
1. Problem and Objective
2. Vision & Technology Review
3. Status Update & Feasibility Study
  1. Parallel Embedded Processor Approaches
  2. Application Specific Hardware Approaches

- Full AC Load Flow Contingency Analysis
- Benchmark data
  - Pentium IV (2.6 GHz, )
    - 7,917 bus: 385 ms per iteration [using WSMP solver - <http://www.alphaworks.ibm.com/tech/wsmp>]
    - 5 iterations per contingency
    - 14,000 contingencies take 7 ½ hours
- Goal
  - Obtain 1 to 2 orders of magnitude improvement within reasonable cost constraints

- Supercomputer in a box
  - PC + SoC (System-on-a-Chip)
  - Massive number of simple processors (200 Processors)
  - Application specific hardware
  - Specialized to power system computation
- FPGA vs. ASIC
  - FPGA provides programmable HW and short design time
  - Embedded processor cores
  - 50-300 MHz vs. 1-2 GHz
  - 3-10 vs. 20+ Processing Units

- Alternate approaches prototyped
  - Tsunami board (Drexel): 5 Altera Stratix
  - Annapolis WildStar (NJIT): 2 Xilinx Virtex II
- Parallel Embedded Processor
  - Parallel Contingency Analysis
  - Parallel Sparse Solver
  - SIMD Processor
- Application Specific Hardware
  - Floating-point Units
  - Matrix Multiplication
  - LU Decomposition
  - Hardware Sparse Solver

# Multi-Embedded Processors for Contingency Analysis



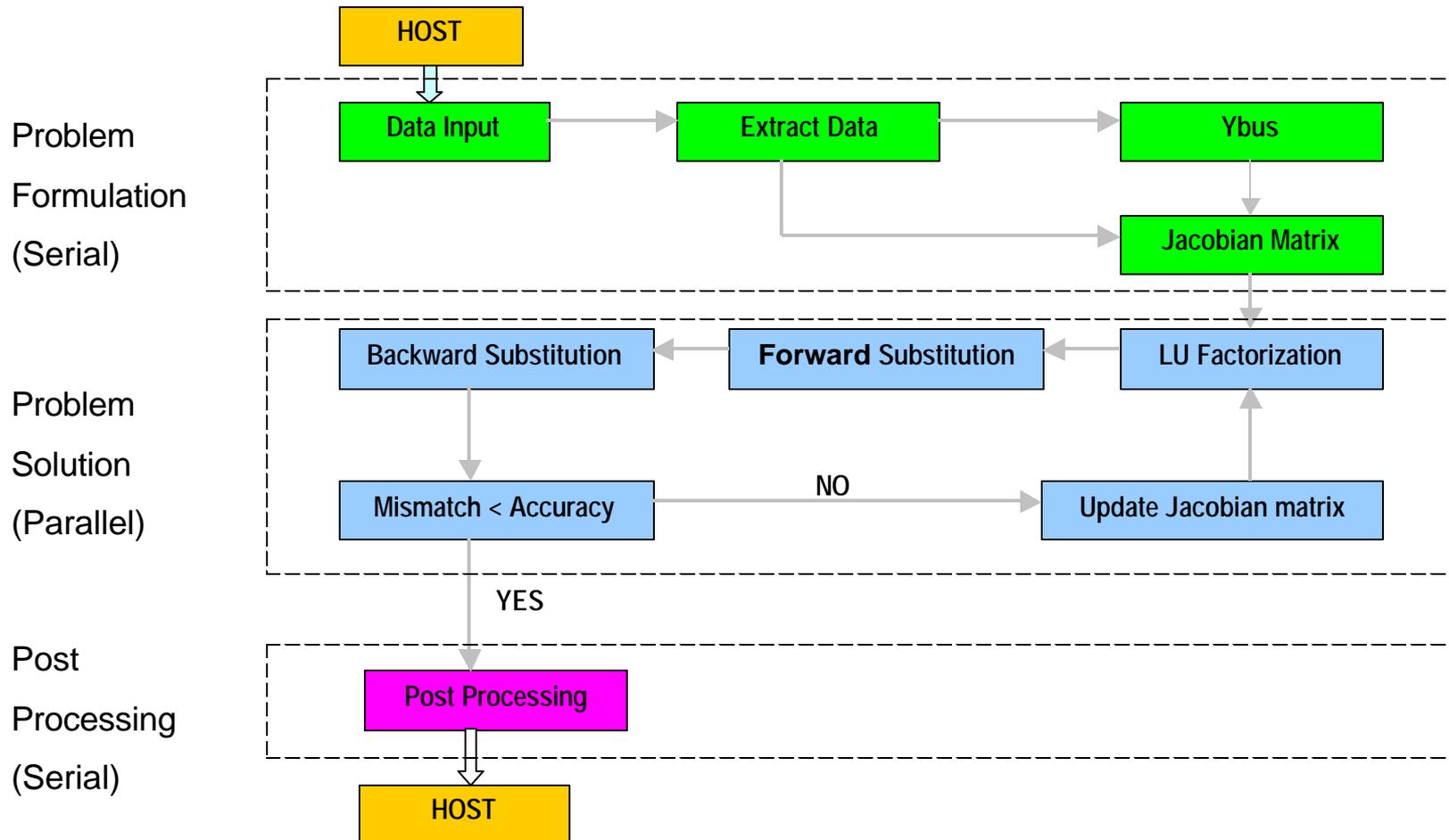
PCI Bus

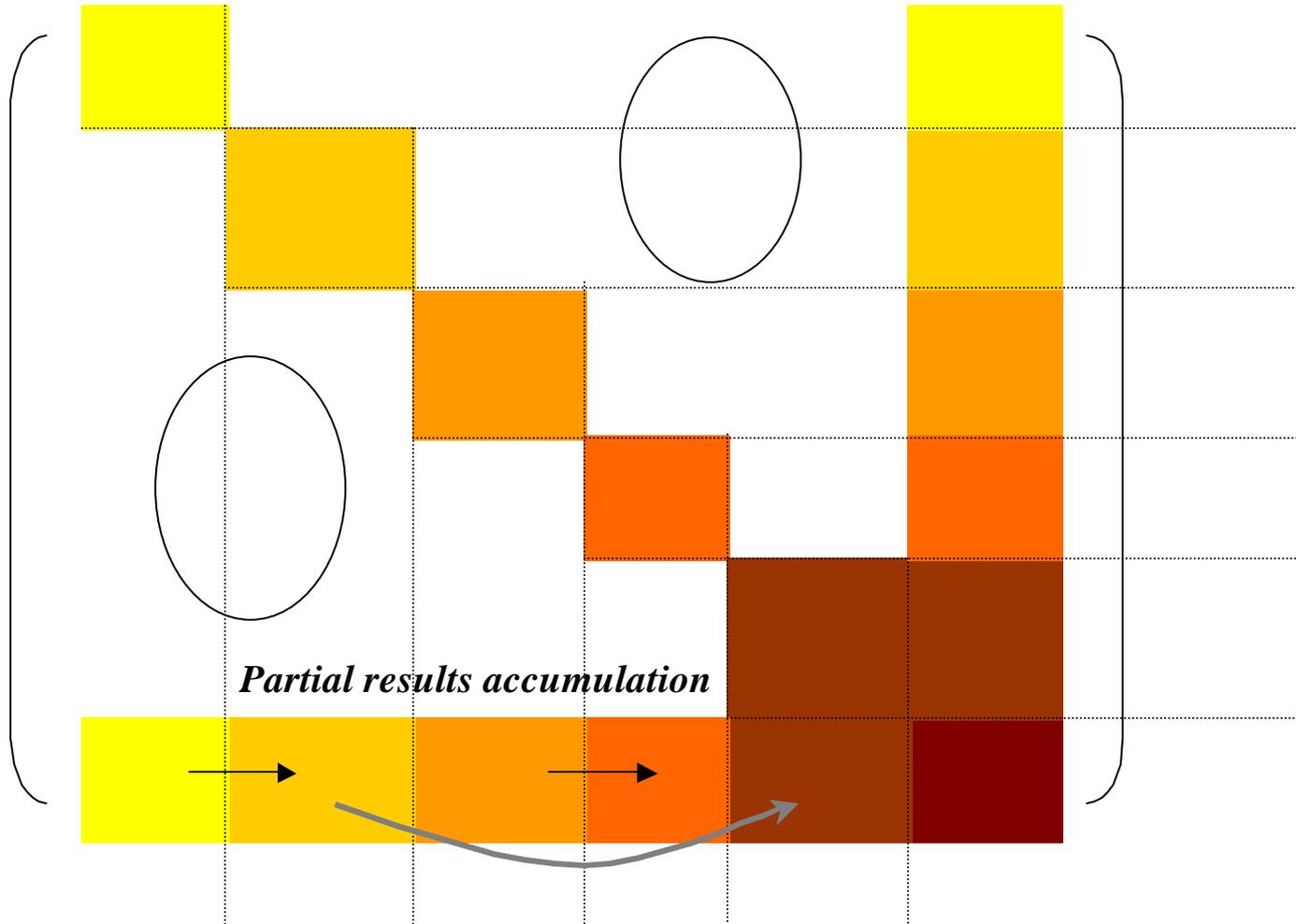


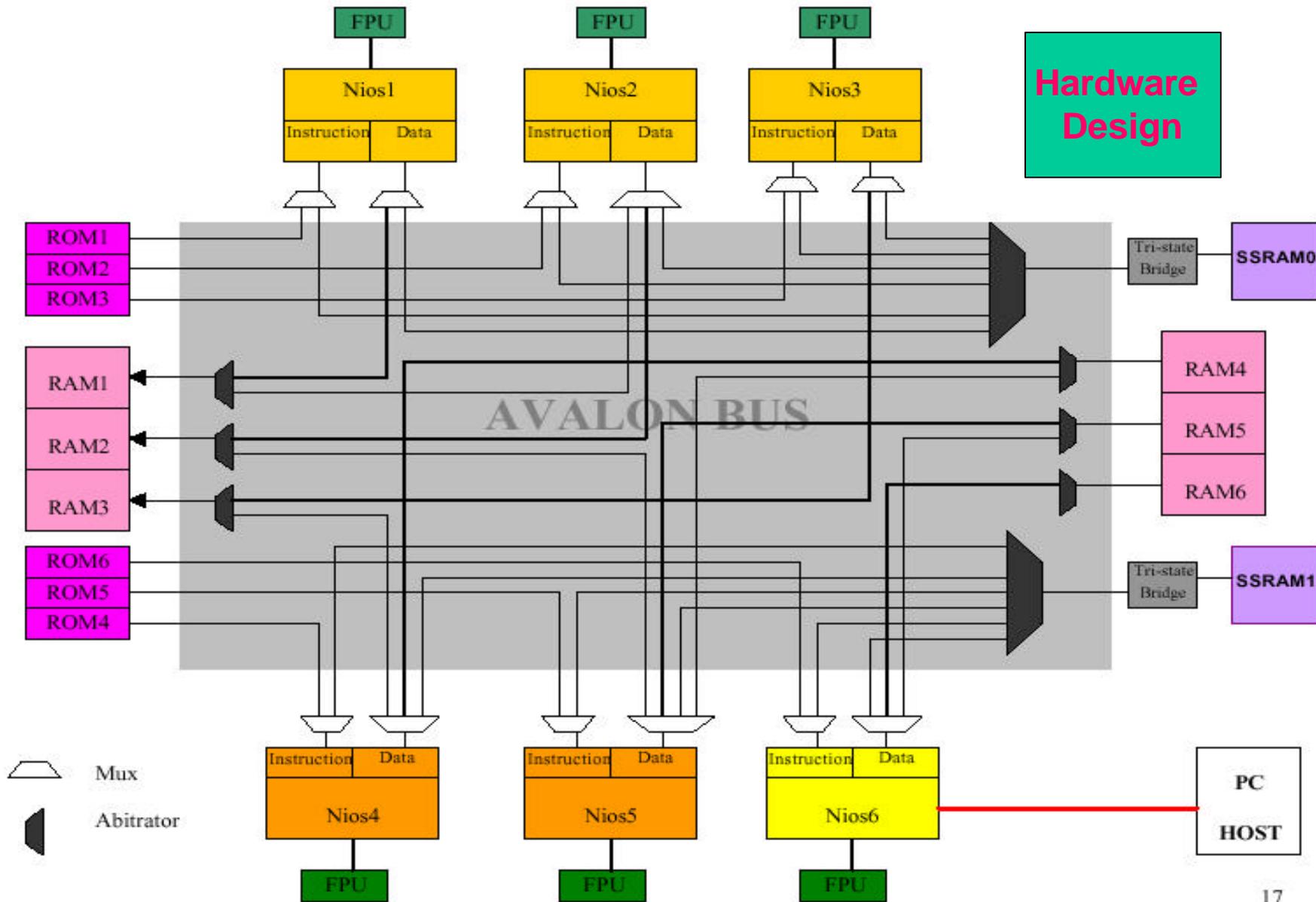
Tsunami  
Board



# Power-Flow Solution Implementation in Hardware

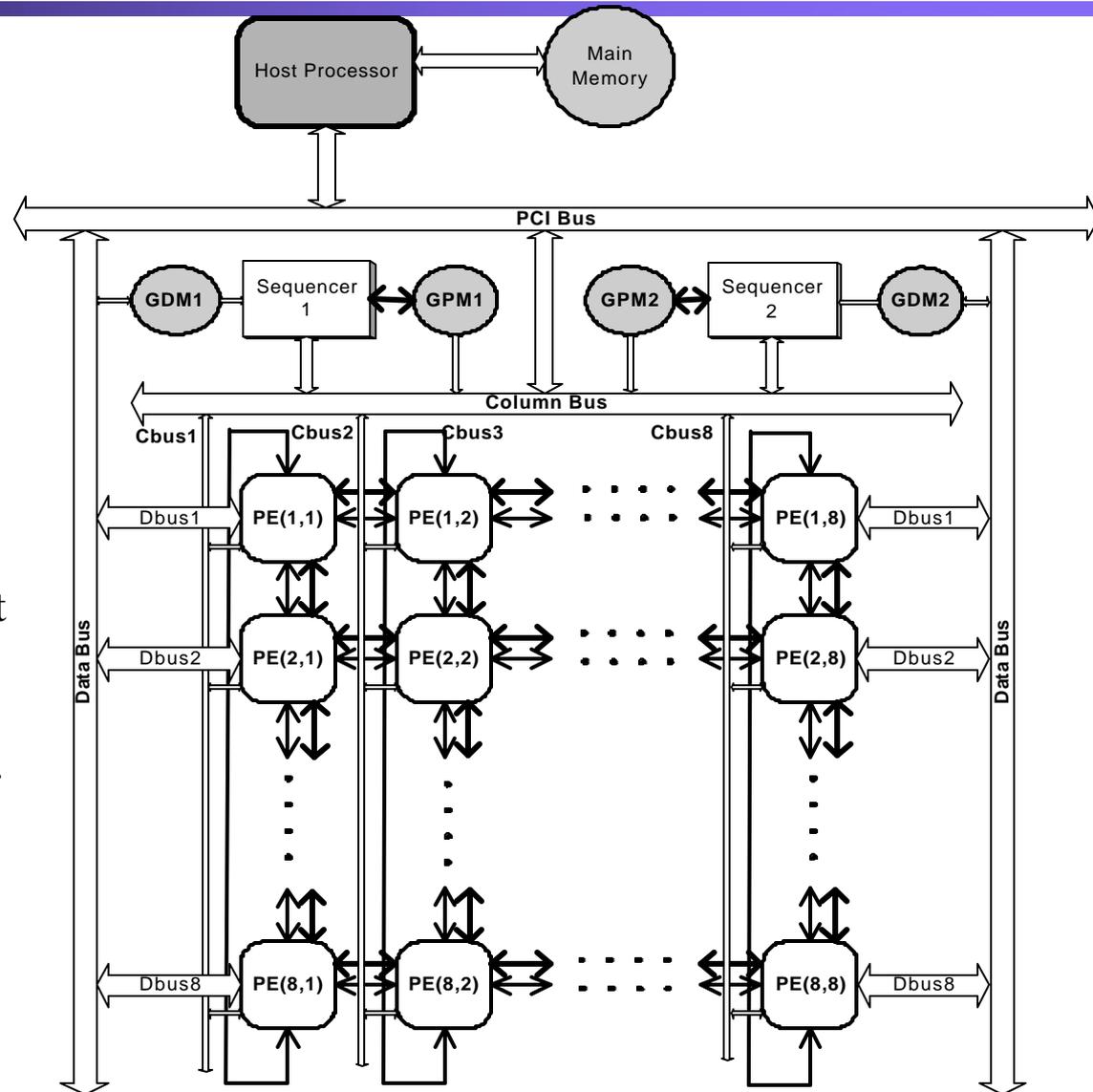


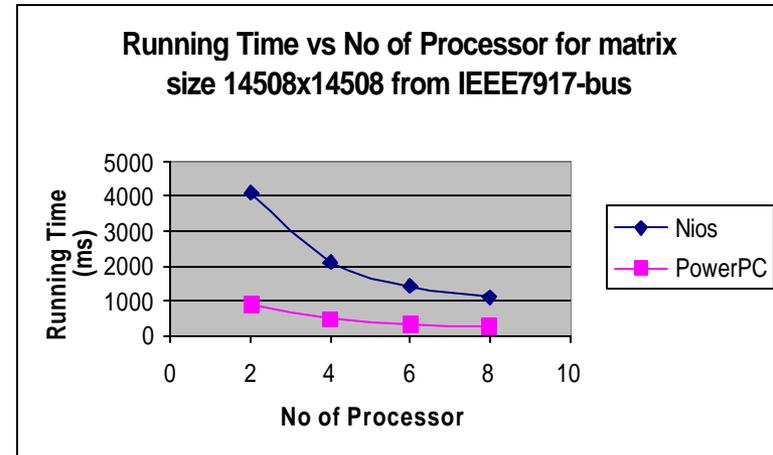
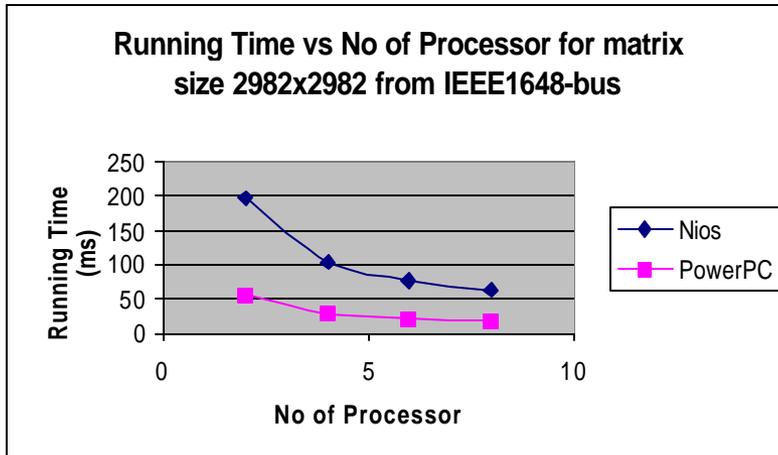




**Hardware Design**

- Implemented on Annapolis WildStar PCI-II board (populated with two FPGAs)
- Local NEWS (North, East, West, South) between PE neighbors
- Two-level global buses
- Column wraparound connection
- PCI communication with host machine
- Customizable in terms of PE function and the total number of PEs





- Nios embedded processors on Altera Stratix FPGA, running at 80 MHz

- 8 processors:

- 1648-bus: 64.179 ms
    - 7917-bus: 1106.676 ms

- 400 MHz PowerPC on Xilinx Virtex 2 FPGA with 80 MHz FPU

- 8 processors:

- 1648-bus: 18.992 ms
    - 7917-bus: 256.382 ms

# Execution Times for Power Flow Analysis with 5 Processors

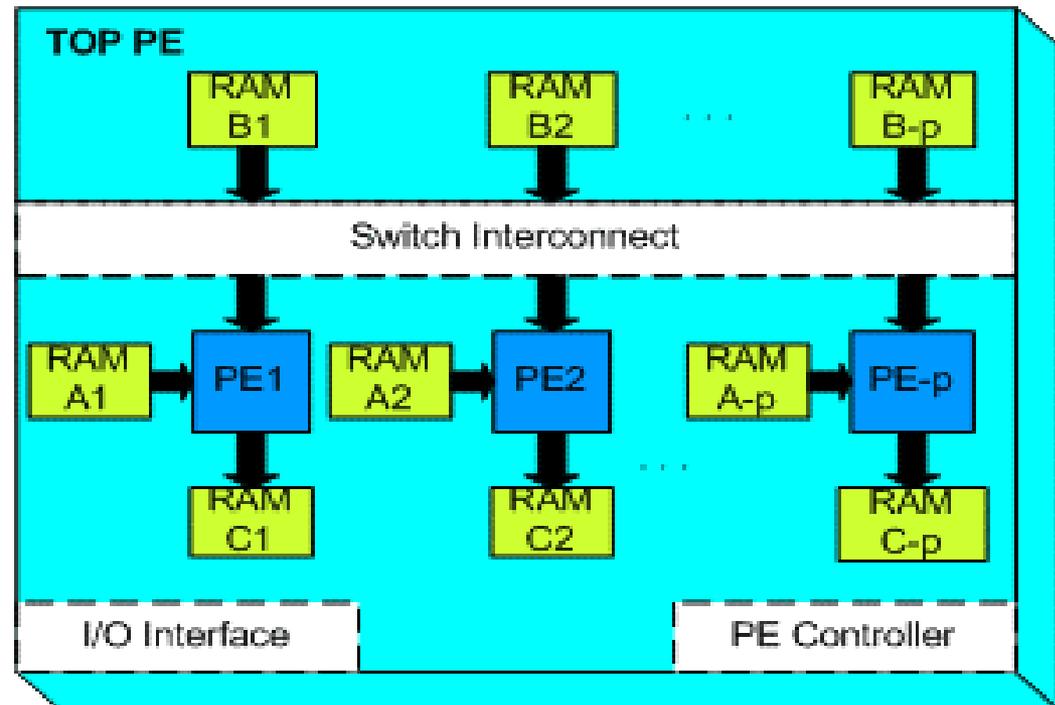
IEEE test systems	30-bus	57-bus	118-bus	300-bus
Iterations	3	4	4	5
Total time (ms)	21.276	89.992	253.148	2545.32
Uni-processor (ms)	66.381	287.074	858.172	10841.55
Speedup	3.12	3.19	3.65	3.97

1. Tolerance: 0.001 p.u.

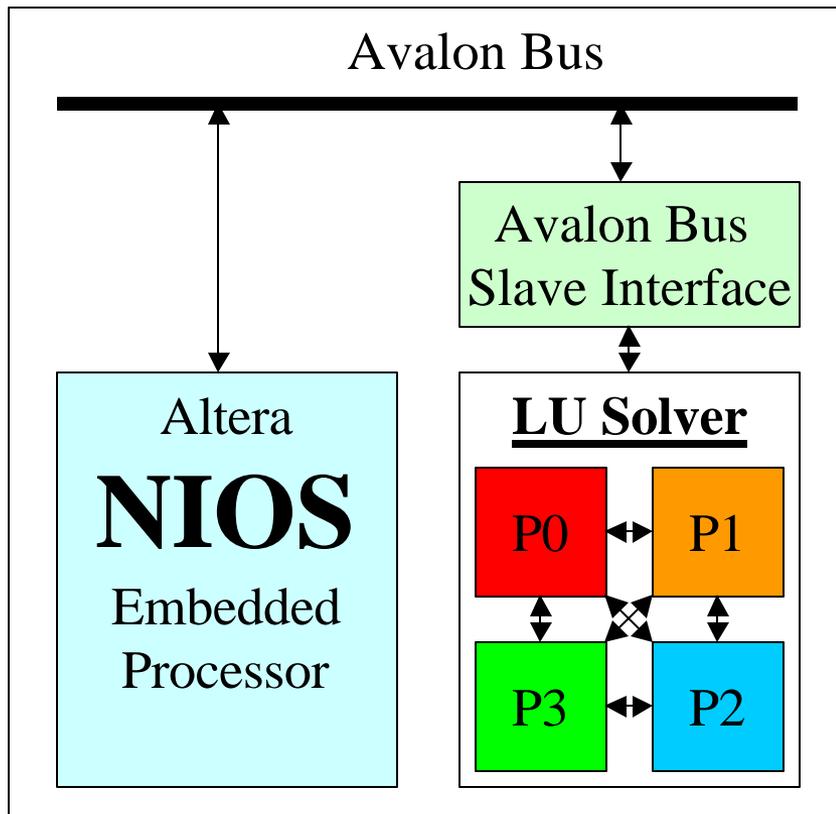
Core	FPGA	fpADD		fpMUL		fpDIV	
		$f_{\max}$ (MHz)	Latency	$f_{\max}$ (MHz)	Latency	$f_{\max}$ (MHz)	Latency
Quixilica	Virtex II	137	10	138	7	139	27
DCD	Virtex II	85	5	74	7	57	15
DCD	Stratix	110	5	86	7	75	15
Nallatech	Virtex II	164	6	127	14	163	26
Drexel	Stratix	173	5	206	4	66	9

- DCD: Digital Core Design
- Virtex II and Stratix are products of Xilinx and Altera respectively
- Latency is the number of clock cycles until solution is valid
- The cores are pipelined allowing for the data to be applied every clock cycle.

- The TOP PE contains ‘p’ number of processing elements (PE)
- Each PE performs a block matrix multiplication with rotating B blocks
  - $MEM-C(i) = MEM-A(i)*MEM-B(k)$
  - Where  $k = 1, 2, 3, \dots p$
- Ex:
  - # PE: 4
  - Matrix Size: 64x64
  - 50MHz
  - Simulation:
    - 68617 clks
    - 1.372 ms
  - Hardware:
    - 68664 clks
    - 1.373 ms



## Stratix 1S25 FPGA

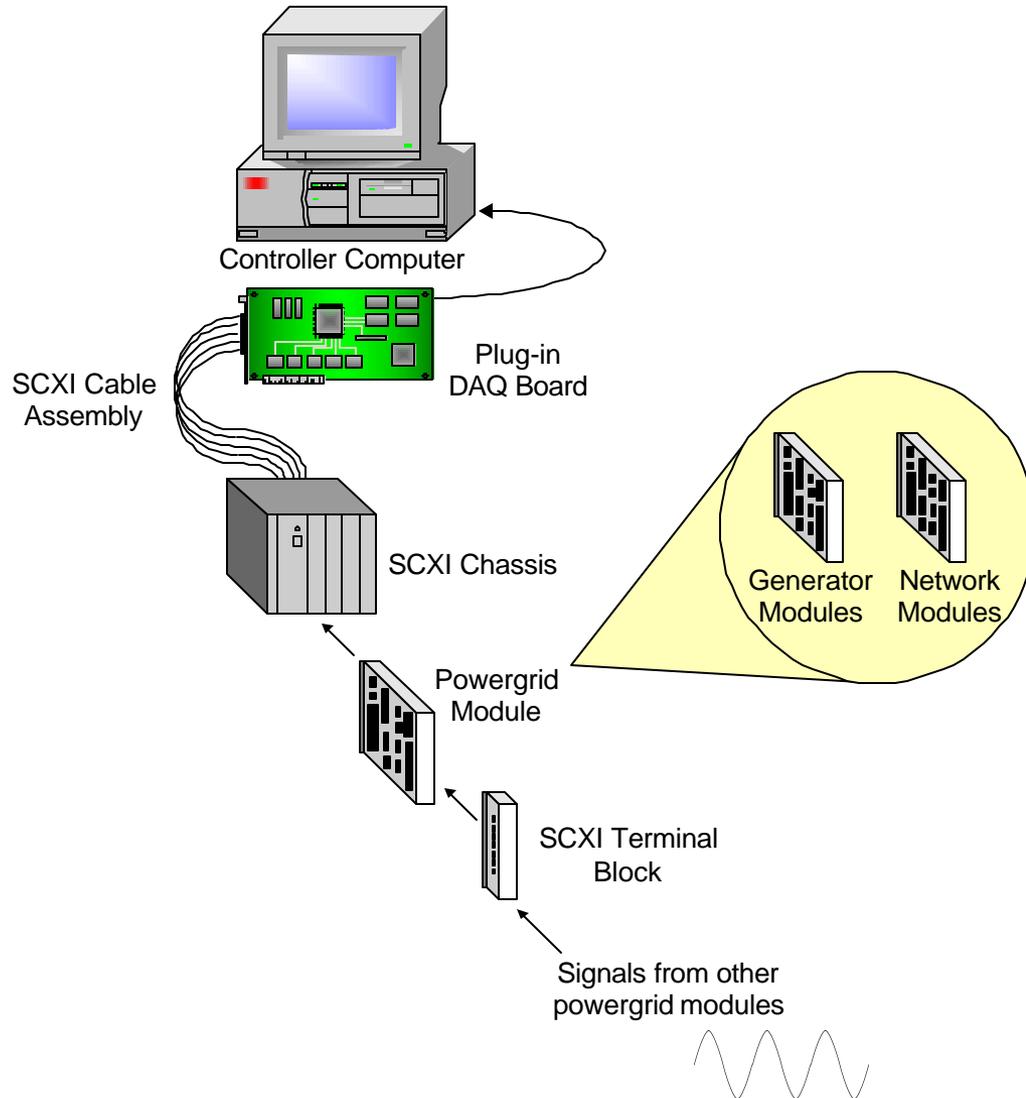


- NIOS processor is used as I/O for LU Solver
- One Stratix 1S25 FPGA can contain a NIOS processor and upto 4 processing elements

- Prototype implementations developed using FPGA
  - Parameterized scalable designs
  - Current embedded processor performance limited due to NIOS + Avalon bus
  - Need high performance processor cores [e.g. PowerPC], high end FPGA devices [e.g. stratix S80], and scalable parallel algorithms
  - Application specific hardware approach shows promise and complete loadflow solution using this approach is under development
  - May need ASIC to achieve desired performance

# PowerGrid Project – Analog Approach

All-Analog System Approach to  
Large-scale Power System Analysis



- Identified key issues in computation “by analog” approach – at both model and emulation levels
- Obtained Initial Design of PC-Board  
Implementation of Prototype
- Performed preliminary benchmark selection and specification as well as software packages for testing

- View of Power system as a single system comprising of a **reconfigurable** interconnection of devices. Initial devices will be generators, lines and loads.
- Emulation of steady state behavior can be obtained by two paths – **static and dynamic**

# Key Modeling Component

## Reconfigurable Power System on Chip (PSOC)

Reconfigurable  
**Analog** hardware

Reconfigurable  
Digital hardware



Operational Transconductance Amplifier (**OTA**) is the key to realize the **reconfigurable** analog hardware.

Sample OTAs:

LM13700 (National Semiconductors), CA3280 (Intersil),  
LT1228 (Linear Technology), MAX435/436 (MAXIM),  
NE5517 (Philips), OPA660 (Burr-Brown)

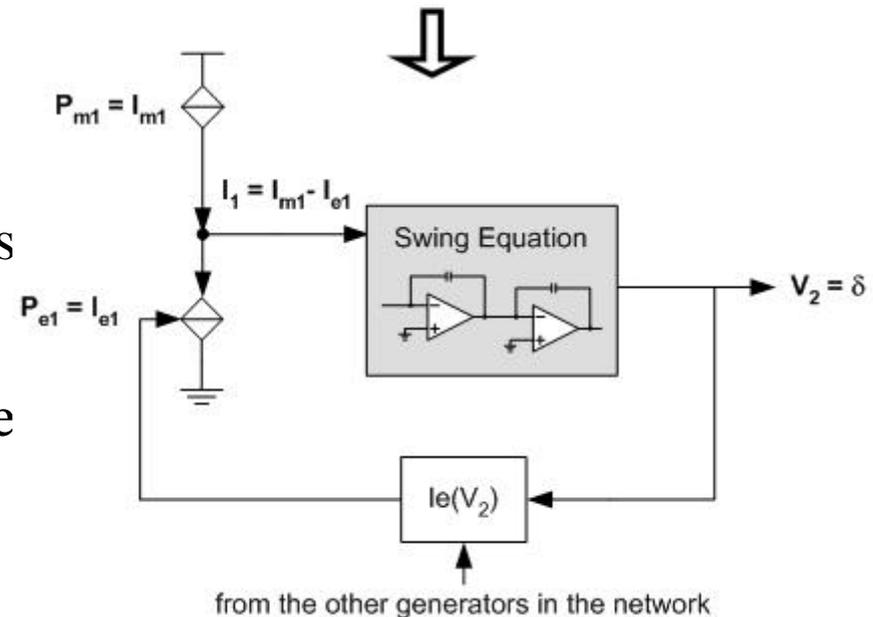
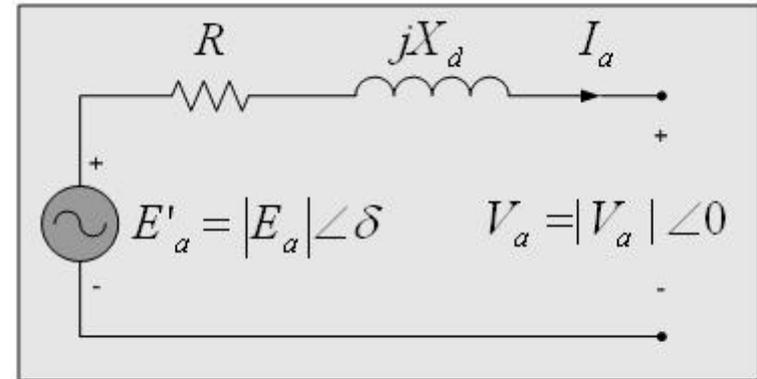
## Steady State

One phase of an AC generator can be modeled as an AC voltage source  $E'_a$

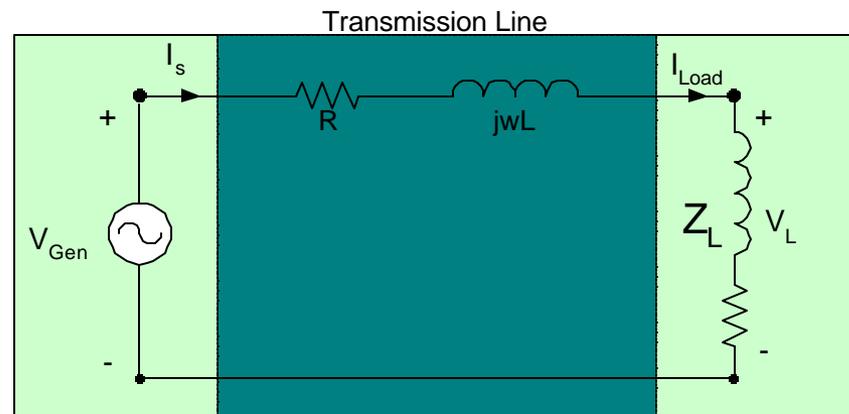
$E'_a$  feeds the current  $I_a$  against the terminal voltage  $V_a$  through an internal impedance

The impedance consists of the stator winding resistance  $R$  and the direct-axis synchronous reactance  $X_d$

To further simplify the circuit, since the stator winding resistance is relatively very small, it can be neglected

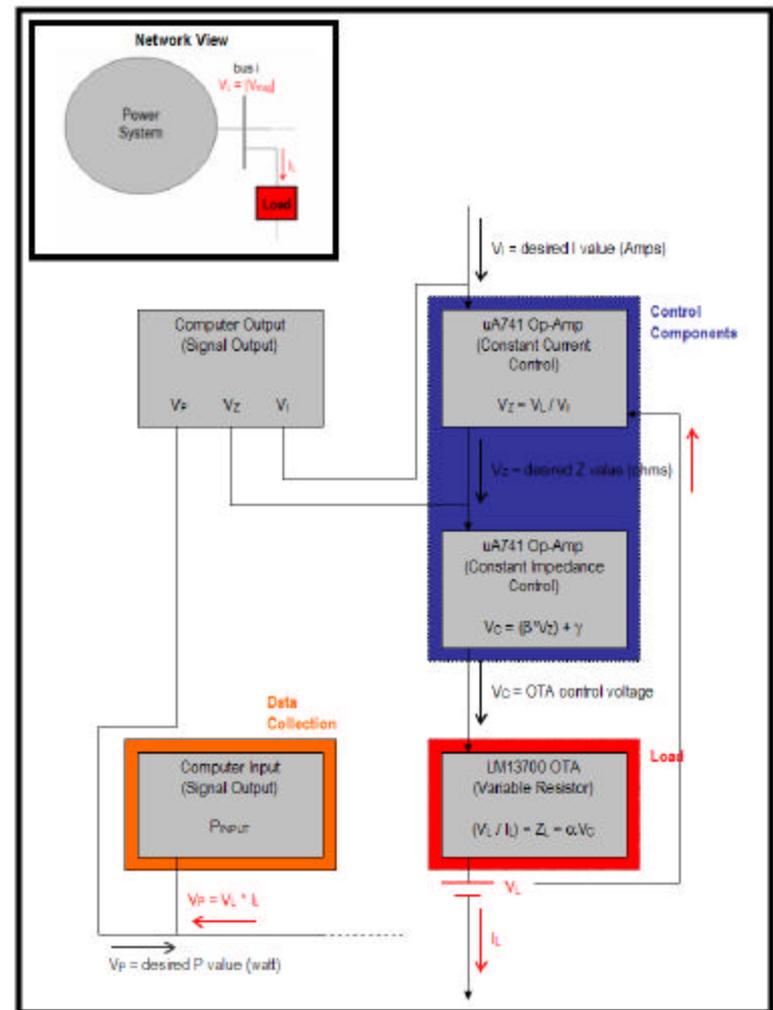


- Analog circuit approach for steady state solution:
  - DC resistive networks broken up into real and imaginary components model transmission lines
  - OTA's utilized as variable resistors to adjust transmission line parameters
  - Lossy line model complete neglecting shunt admittance (constant current/constant impedance loads.
  - 3-bus power system prototype is being designed and constructed
  - The speed, accuracy, and scalability of hardware prototype will be analyzed

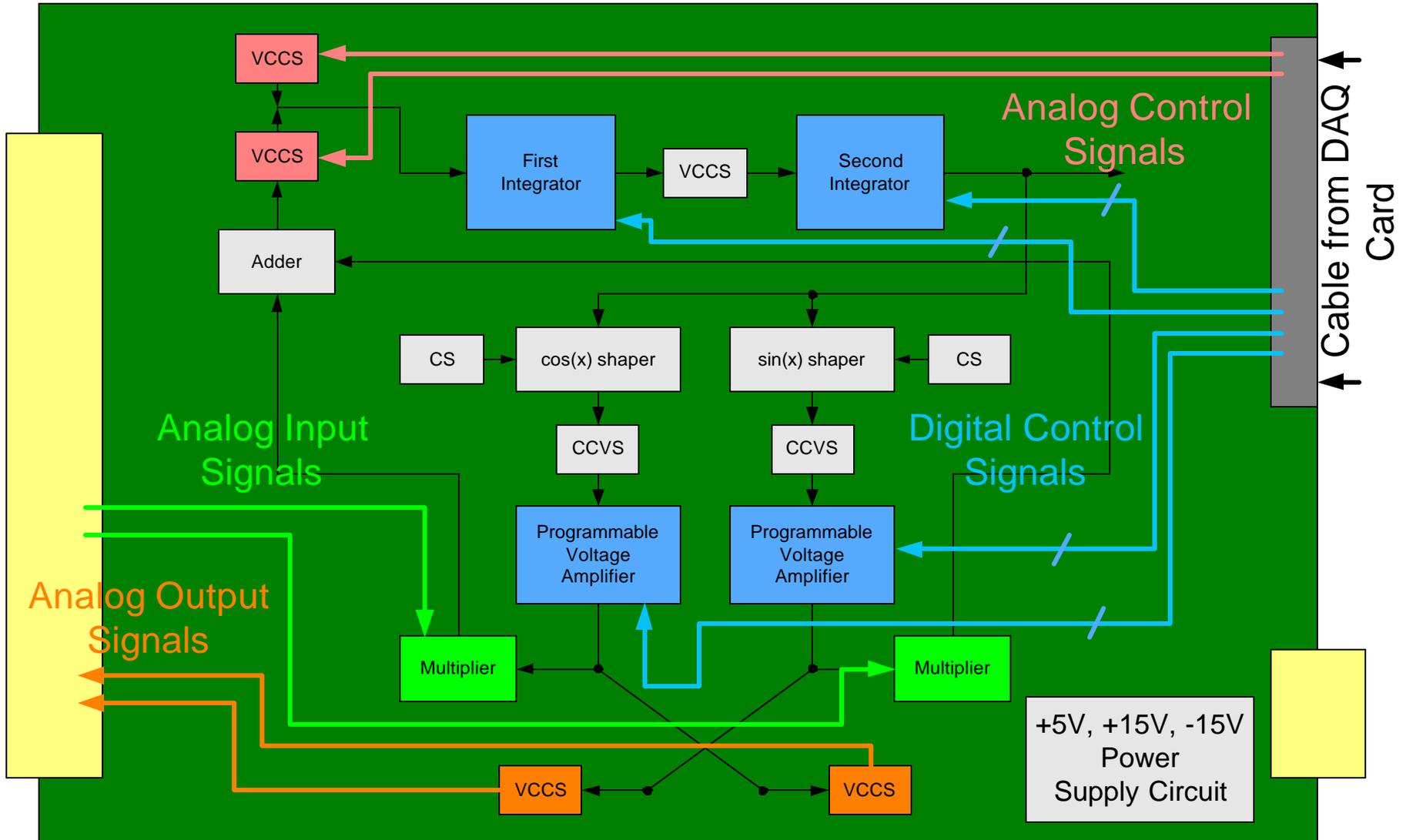


# Power System Load Model

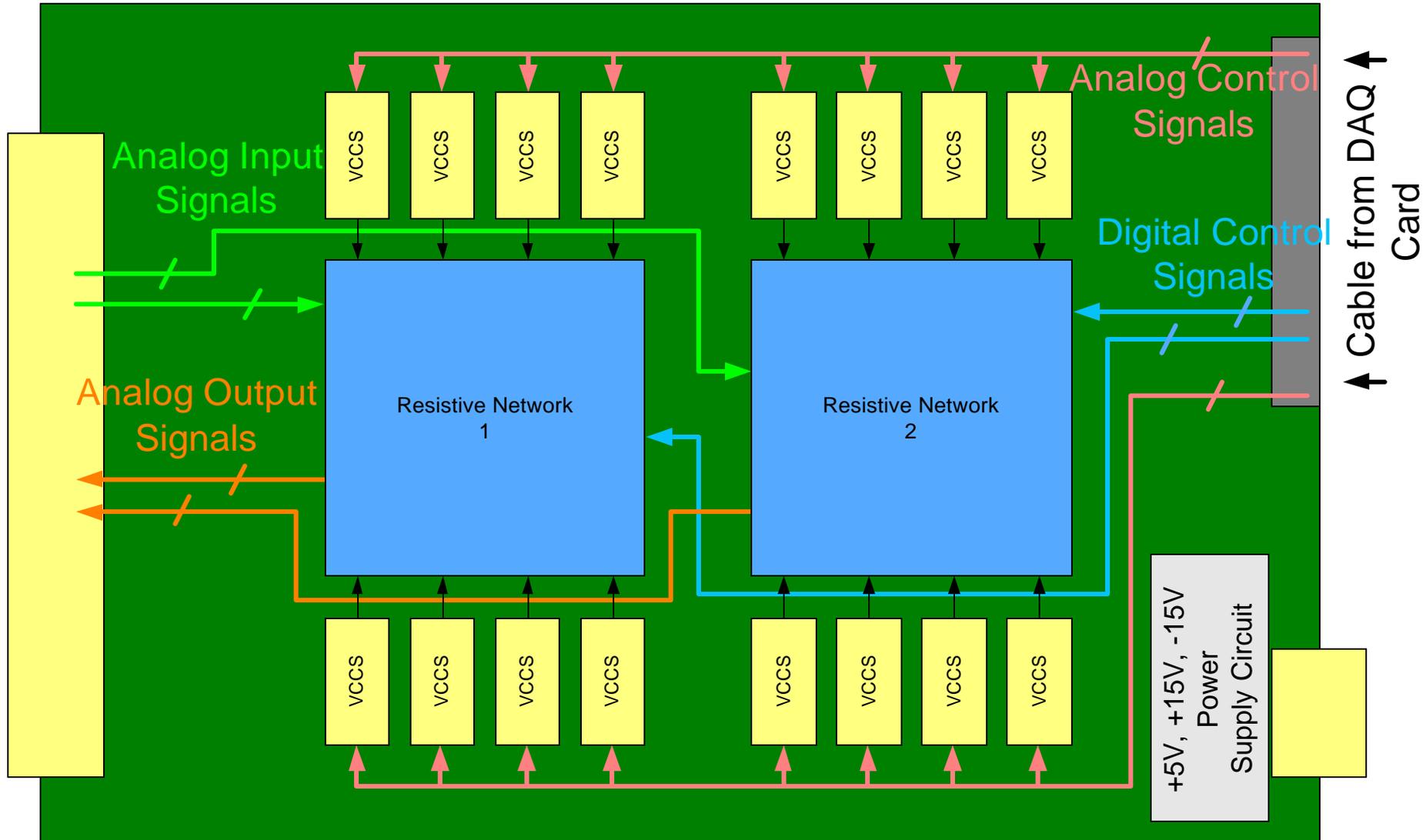
- Progress
  - In process of completing load hardware simulation in PSPICE.
  - Two Levels
    - Network View (top)
    - Component Level (rest)
- Future Work
  - Build and test hardware implementation
  - Analyze speed, accuracy, and scalability of design



# Generator Module - Showing Digital / Analog Control Signals

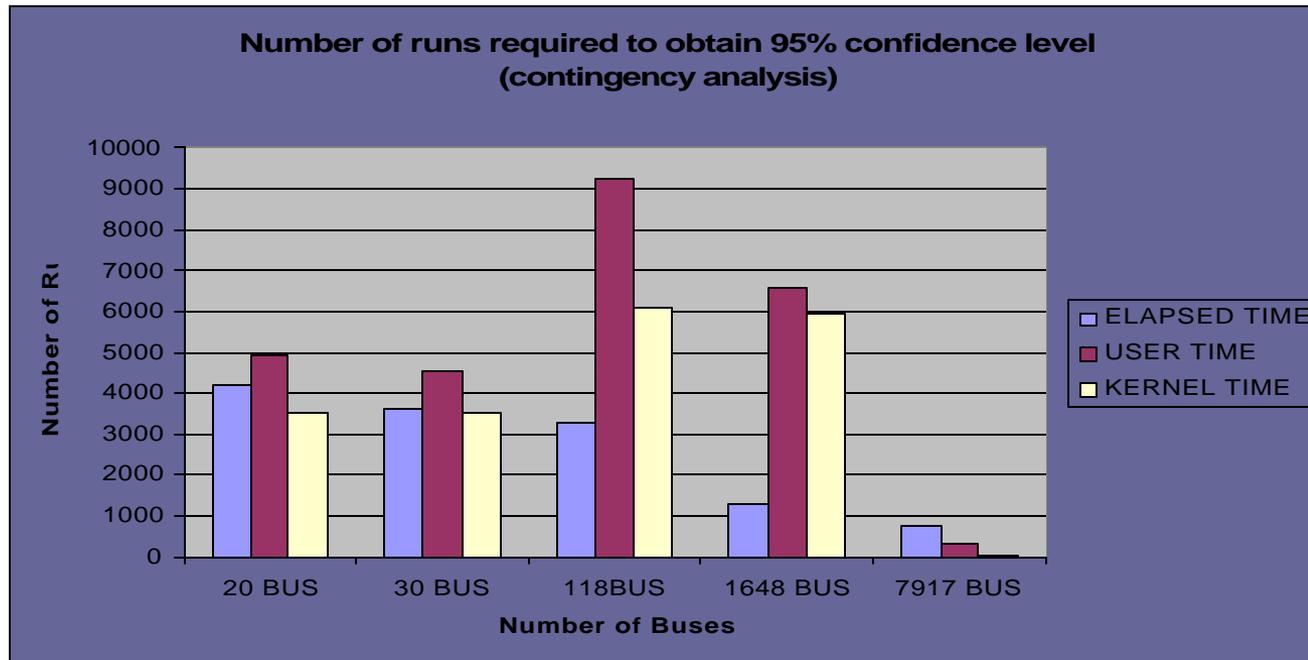


# Network Module - Showing Digital / Analog Control Signals



## STATISTICAL ERROR ANALYSIS

- The main objective is to provide in house benchmarking using a variety of systems
- The error analysis was performed on data obtained from the PSS/E package
- The calculation below indicates that that if the same experiment is repeated many times (taking a new random sample each time) and if the sample size is 1274 and the acceptable error is 0.01 then about 95% of the time the null hypothesis is correctly rejected
- The acceptable errors considered in these calculations vary according to the mean time required to solve the system



## FUTURE WORK:

- Benchmarking for Analog Simulation studies
- Survey of programming tools available for study of analog simulations
- Testing for computational speed and accuracy

## Papers

“High-Performance Linear Algebra Processor using FPGA”, J. R. Johnson, P. Nagvajara, C. Nwankpa, HPEC 2003, Seventh Annual Workshop on High Performance Embedded Computing, Sept. 23-25, 2003, MIT Lincoln Laboratory

“VLSI Based Analog Power System Emulator for Fast Contingency Analysis”, S. P. Carullo, M. Olaleye, C. Nwankpa, HICSS-37, 37th Annual Hawaii International Conference on System Science, Jan. 5-8, 2004, Waikoloa, Hawaii

- Analog Approach Prototype
  - Development of PC-Board Based Generator Module
  - Development of PC-Board Based Network Module
  - Drexel focuses on Multiprocessor + Application Specific HW
  - Developed appropriate signal conditioning and data acquisition schemes for modules
- Benchmarking study
  - Report on correctness testing and quality of solutions
- Scalability analysis

1<sup>st</sup> Quarter: Sep.1, 03 – Nov. 31, 03

1. Model development of generators, lines and loads
2. Evaluation of Computational Speed and Accuracy.

2<sup>nd</sup> Quarter: Dec. 1, 04 – Feb. 29, 04

1. Hardware Prototype Design
2. Power System Analysis: Speed and Accuracy Issues
  - For both Steady State and Dynamic analysis

3<sup>rd</sup> Quarter: Mar. 1, 04 – May. 30, 04

1. Analog Hardware Implementation
2. Evaluation

4<sup>th</sup> Quarter: Jun. 1, 04 – Aug. 31, 04

## 1. Scalability Analysis

- Estimates on computation requirements
- Signal conditioning and data acquisition dependencies